UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,539	04/15/2002	Anand S. Murthy	42390.P6624PCT	6105

7590 03/13/2003

Blakely Sokoloff Taylor & Zafman
12400 Wilshire Blvd Seventh Floor
Los Angeles, CA 90025

EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,539	MURTHY ET AL.	
	Examin r	Art Unit	
	Brook Kebede	2823	

-- Th MAILING DATE of this communication appears on the cover sh et with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicants' affirmation telephonic election of claims 11-30 **with traverse** in Paper No. 8 is noted. Although applicants were indicating cancellation of the non-elected claims, i.e., claims 1-10, in the remark filed on December 17, 2002, applicants were not amended the claims that authorizes the Office to cancel the non-elected claims. Furthermore, applicants' election of claims 11-30 in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election **without traverse** (MPEP § 818.03(a)).

2. Claims 1-10 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 8.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 11-13 and 22-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (JP/63076481).

Re claim 11, Horiuchi et al. disclose a method of making a junction, comprising: forming a patterned structure on a surface of a substrate (see Fig. 3B), the substrate (1) being of a first conductivity type; isotropically etching the substrate (1) such that a recess in the substrate is formed, the recess (not labeled) including a portion that underlies the patterned structure, the

recess having a surface; and selectively forming a layer of a first material (91 101) having a second conductivity type in the recess (see Figs. 3B-3D).

Re claim 12, as applied to claim 11 above, Horiuchi et al. disclose all the claimed limitations including the limitation prior to selectively forming the layer of the first material (91 101), selectively forming a layer of a second material (9 10) having the first conductivity type over the surface of the recess (see Figs. 3B-3D).

Re claim 13, as applied to claim 12 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon, and the second material comprises doped silicon (see Figs. 3B-3D).

Re claim 17, as applied to claim 11 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein the patterned structure comprises a dielectric layer and a conductive material disposed over the dielectric layer (see Figs. 3B-3D).

Re claim 18, as applied to claim 11 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein etching passivates the surface of the recess (see Figs. 3B-3D).

Re claim 19, as applied to claim 11 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein etching comprises exposing the substrate to SF6 and He in an R-F plasma etching system (see Figs. 3B-3D).

Re claim 20, as applied to claim 11 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein forming the first material comprises epitaxially depositing a layer of crystalline material (see Figs. 3B-3D).

Re claim 21, as applied to claim 11 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein forming the first material comprises epitaxially depositing a layer of crystalline material; and forming the second material comprises epitaxially depositing a layer of crystalline material; wherein the substrate remains unexposed to the atmosphere subsequent to forming the first material and prior to forming the second material (see Figs. 3B-3D).

Re claim 22, Horiuchi et al. disclose a method of making a transistor, comprising: forming a dielectric (3) on a first surface of a wafer (1); forming a conductive layer (4) overlying the dielectric (3); patterning the conductive layer (4) and dielectric (3)so as to form a gate structure (see Fig. 3B); forming recesses (not labeled) adjacent and partially subjacent the gate structure(3 4 5 18); and in a continuous operation, back filling the recesses with doped crystalline material (9 10); wherein back filling comprises forming crystalline material of at least a first conductivity type (see Figs. 3B-3D).

Re claim 23, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein the crystalline material of the first conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium (see Figs. 3B-3D).

Re claim 24, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein back filling further comprises forming crystalline material of a second conductivity type (see Figs. 3B-3D).

Re claim 25, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein the crystalline material of the second conductivity

type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium (see Figs. 3B-3D).

Re claim 26, as applied to claim 25 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein back filling comprises a selective deposition (see Figs. 3B-3D).

Re claim 27, Horiuchi et al. disclose a method of fabricating a FET, comprising: forming a gate electrode having side walls over a gate insulator on a surface of a semiconductor substrate having a first conductivity type; forming first spacers along the sidewalls of the gate electrode; forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface; substantially filling the recess with a fist layer of doped crystalline material, the first layer having a second conductivity type (see Figs. 3B-3D).

Re claim 28, as applied to claim 27 above, Horiuchi et al. disclose all the claimed limitations including the limitation further comprising depositing the first layer of doped crystalline material until a vertical distance between a top surface of the first layer and the surface of the substrate is greater than a vertical distance between a top surface of the gate insulator and the surface of the substrate (see Figs. 3B-3D).

Re claim 29, as applied to claim 27 above, Horiuchi et al. disclose all the claimed limitations including the limitation forming a second layer of doped crystalline material over the substrate surface of the recess, the second layer having the same conductivity type as the semiconductor substrate, and the second layer having a doping concentration that is greater than a doping concentration of the semiconductor substrate near the substrate surface of the recess (see Figs. 3B-3D).

Re claim 30, as applied to claim 29 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein forming a recess comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1. 1 cm, an RF power in the range of approximately 50 W to 200 W, a pressure greater than approximately 500 mT, and plasma etching with sulfur hexafluoride and helium (see Figs. 3B-3D).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (JP/63076481) in view of Chau et al. (US/6,165,826).

Re claim 14, as applied to claim 12 above, Horiuchi et al. disclose all the claimed limitations. Although it is well-known in the art to from doped SiGe using a solid phase epitaxy to form buried source and drain region, Horiuchi et al. do not specifically disclose a first material

comprises doped silicon germanium, and the second material comprises doped silicon germanium.

Chau et al. disclose forming of doped silicon-germanium in the recess to form buried source drain junction (see Fig. 5D). As Chau et al. disclose, silicon-germanium semiconductor material is preferred because it exhibits good selectivity to silicon during deposition and exhibits many microscopic "faults" and "dislocations" which enhances in the solid diffusion of dopants through the semiconductor material (see Col. 8, lines 46-67 and Col. 13, lines 25-42).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Horiuchi et al. reference with silicon-germanium layer as taught by Chau et al. because the silicon-germanium would have provided superior material since it exhibits good selectivity to silicon during deposition and exhibits many microscopic "faults" and "dislocations" which enhances in the solid diffusion of dopants through the semiconductor material.

Re claim 15, as applied to claim 14 above, Horiuchi et al. and Chau et al. in combination disclose all the claimed limitations including the limitation wherein the second material has a thickness that is less than a thickness of the first material (see Figs. 3B-3D).

Re claim 16, as applied to claim 15 above, Horiuchi et al. and Chau et al. in combination disclose all the claimed limitations including the limitation wherein the first material has a top surface that is above a plane defined by the surface of the substrate (see Figs. 3B-3D).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Chau et al. (US/5,908,313), Wu (US/5,994,747), and Deleonibus (US/6,091,076) also disclose similar inventive subject matter.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
March 8, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800